September 2021

MICROPROCESSOR

Time Allowed: 1.5 Hours *Full Marks: 70*

Answer to Question No.1 is compulsory and Answer <u>any two</u> questions from the rest.

1. Answer the following questions (any twenty): 2x20

i) This signal indicates that another master is requesting the use of the address and data buses –
a) READY, b) HOLD, c) HLDA, d) INTA.

ii) The 8-bit flag register of 8085 microprocessor is responsible to indicate – a) The condition of result of Arithmetic and Logical operations, b) The condition of memory, c) The result of addition, d) The result of subtraction.

iii) _____is also a 16-bit register works like stack, which is always incremented/decremented by 2 during push & pop operations.

iv) If 'n' denotes the number of clock cycles and 'T' denotes period of the clock at which the microprocessor is running, then the duration of execution of loop once can be denoted by–
a) n+T, b) n-T, c) n*T, d) n/T.

v) If a microprocessor uses a 5 MHz oscillator. The duration of one T state is –
a) 1 μs, b) 0.33 μs, c) 2 μs, d) 0.2 μs.

vi) In which of these modes, the immediate operand is included in the instruction itself–a) Register operand mode, b) Immediate operand mode, c) Register and immediate operand mode, d) None of the mentioned.

vii) Which addressing mode execute its instructions within CPU without the necessity of reference memory for operands –a) Implied Mode, b) Immediate Mode, c) Direct Mode, d) Register Mode.

viii) OUT 80 is the example of 3-byte instruction – a) True, b) False

ix) Which interrupt is not level sensitive in 8085? –a) RST6.5 is a raising edge-trigging interrupt,
b) RST7.5 is a raising edge-trigging interrupt, c) Both a & b, d) None of the above.

x) In memory-mapped scheme, the devices are viewed as – a) Distinct I/O devices, b) Memory locations, c) Only input devices, d) Only output devices

xi) The 8085 microprocessor has two instructions for data transfer between the processor and the I/O devices – a) MVI & STA, b) Rx & Tx, c) DIN & DOUT, d) IN & OUT.

xii) In input interfacing _____ is used as an interfacing port.

xiii) During I/O Write Machine Cycle(Specifically in T2), value of the following signals are –
a) IO/M'=1,RD=0,WR=1,IO/W=1, b) IO/M'=1,RD=1,WR=0,IO/W=0,
c) IO/M'=1,RD=1,WR=0,IO/W=1, d) IO/M'=0,RD=1,WR=1,IO/W=1

xiv) _____register must be initialized before any use of 8251.

xv) The signal that may be used either to interrupt the CPU or polled by the CPU is –
a) TXRDY(Transmitter ready), b) RXRDY(Receiver ready output),
c) DSR(active low), d) DTR (active low)

xvi) The asynchronous mode is programmed by mode word format – a) True, b) False

xvii) What must be the contents of the control word of Intel 8255 for Mode 0 (operation) and for the following ports configuration : Port A-output, Port B-output, Port Lower-Output, Port Cupper-input – a) 85H, b) 86H, c) 87H, d) 88 H

xviii) The speciality of the 8253 counters is that they can be easily read on line without disturbing the _____ input to the counter.

xix) In 8279 the sensor RAM acts as 8-byte first-in-first-out RAM in – a) Keyboard mode, b) Strobe input mode, c) Keyboard and strobe input mode, d) Scanned sensor matrix mode.

xx) In 8259 The register that stores all the interrupt requests in it in order to serve them one by one on a priority basis is – a) Interrupt Request Register, b) In-Service Register, c) Priority resolver, d) Interrupt Mask Register.

xxi) BHE of 8086 microprocessor signal is used to interface the – a) Even bank memory, b) Odd bank memory, c) I/O, d) DMA.

xxii) 8088 microprocessor differs with 8086 microprocessor in – a) Data width on the output, b) Address capability, c) Support of coprocessor, d) Support of MAX / MIN mode.

xxiii) In 8086 the overflow flag is set when signed numbers go out of their range after an arithmetic operation –a) True, b) False.

xxiv) The result of MOV AL, 65 is to store –a) Store 0100 0010 in AL, b) Store 42H in AL, c) Store 40H in AL, d) Store 0100 0001 in AL.

xxv) This signal is used as the system clock for devices connected with the microprocessor – a) X1, X2, b) CLOCK IN, c) CLOCK OUT, d) IO/M'.

2. a) Interface a 27128 EPROM (16K*8 bits or 16 KB) IC with the 8085 using a NAND gate address decoder such that the starting address assigned to the chip is C000H.
   b) Compare I/O mapped I/O and Memory mapped I/O. (8+7)

3. a) Define block transfer DMA.
   b) Compare synchronous and asynchronous data transfer.
   c) Explain with neat sketch the interfacing circuit of 8085 and 8251. (3+5+7)

4. a) Explain different modes of 8255.
   b) Draw the functional block diagram of Programmable Counter (8253). (10+5)

5. a) Explain with neat sketch the block diagram of 8086.
   b) Develop an Assembly Language Program to add a data byte located at offset 0500H in 2000H segment to another data byte available at 0600H in the same segment and store the result at 0700H in the same segment. (8+7)

6. a) Define Memory Management.
   b) What will be the status of the flag register of 8086 after ORing operation between 101011111111 and 111110101010?
   c) What is super scalar architecture?
   d) Define protected virtual address mode. (3+6+3+3)

7. a) Define addressing mode of 8086.
   b) What are the advantages of Multi User Operating System?
   c) What are the different types of interrupt available in 8086? (8+3+4)

8. a) Define features of 8085.
   b) Explain with neat sketch the bus organization of 8085.
   c) Describe different timing and control signal of 8085. (3+6+6)

9. a) Draw the timing diagram of LHLD, 16-bit address.
   b) Define Bus idle cycle. (10+5)

10. a) Define the instructions set according to size.
    b) Develop an Assembly Language Program to find the largest number in an array.
    c) Define Stack Memory. (5+7+3)

11. Write short notes on: (Any two)
    a) SIM
    b) PSW
    c) Opcode Fetch (7.5+7.5)